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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/652,790	08/29/2003	Masanori Minamio	10873.1294US01	3411

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EXAMINER	
TRAN, MAI HUONG C	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/652,790	MINAMIO ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *11-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/28/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Applicant's election with traverse of Group I (claims 1-10) drawn to a semiconductor device is acknowledged. Accordingly, claims 11-13 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Because Applicant did not distinctly and specifically point out the supposed error in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-2 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,337,510 to Chun-Jen et al. (hereinafter Chun-Jen).

Regarding to claim 1, figure 1 of Chun-Jen discloses a lead frame comprising a frame (col. 2, line 38, col. 3, line 1) and a plurality of inner leads 120 extending inward from the frame, wherein each of the inner leads 120 includes a protruded portion 121 provided on a surface of an external side portion thereof, the protruded portion being protruded in a thickness direction (col. 2, lines 34-67, col. 3, lines 1-8).

Regarding to claim 2, Chun-Jen discloses the lead frame wherein a thickness of the protruded portion 121 of each inner lead 120 is substantially equal to a thickness of the frame (fig. 1).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,337,510 to Chun-Jen et al. in view of Suminoe et al. (U.S. 6,380,620) (hereinafter Suminoe).

Regarding to claim 3, Chun-Jen discloses the claimed invention except for the lead frame wherein an insulation tape is stuck on a surface of each protruded portion so that the protruded portion is supported by the insulation tape. However, Suminoe teaches an insulation tape 2 is stuck on a surface of an inner lead 1a so that the inner lead is supported by the insulation tape (col. 8, lines 42-48, and figs. 2(a), 2(b)).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form an insulation tape that is stuck on a surface of an inner lead so that the inner lead is supported by the insulation tape, as taught by Suminoe in order to ensure that deformation due to stress during manufacture is prevented from easily occurring to the inner lead section, thereby resulting in that package defects resulting on the foregoing stress are prevented (col. 4, lines 35-43).

Claims 4-10 and 14 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,337,510 to Chun-Jen et al. in view of Sano et al. (US 5.952,714) (hereinafter Sano) and further in view of Hong et al. (US 6,297,543) (hereinafter Hong).

Regarding to claim 4, figures 1 and 2 of Chun-Jen discloses a semiconductor device comprising a semiconductor chip 110; a plurality of inner leads 120 arranged along a periphery of the semiconductor chip 110; connecting members 130 for connecting the semiconductor chip 110 with the respective inner leads 120; an encapsulating resin 140 for encapsulating surfaces of the semiconductor chip 110 and the

connecting members 130; each of the inner leads 120 extends across the periphery of the semiconductor chip 110 from an internal side to an external side of the periphery, and includes a protruded portion 121 provided on a surface of the inner lead 120 on an external side relative to the periphery of the semiconductor chip 110, the protruded portion 121 being protruded in a thickness direction, conductive bumps 130 that are formed as the connecting members of the semiconductor chip 110 are connected with internal portions 122 of the respective inner leads 120, the internal portions 122 being positioned inward relative to the protruded portions 121 (col. 2, lines 34-67, col. 3, lines 1-19).

Chun-Jen does not disclose a semiconductor chip on a surface of which a group of electrodes is provided; and external electrodes exposed from the encapsulating resin, and the external electrodes are formed on surfaces of the protruded portions, and tip ends of the external electrodes are protruded relative to a back face of the semiconductor chip.

However, Sano discloses a semiconductor chip on a surface of which a group of electrodes 28 is provided (col. 4, lines 59-63, and fig. 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a semiconductor chip on a surface of which a group of electrodes 28 is provided, as taught by Sano in order to form the apparatus to be portable and smaller in size, many of the components are mounted in an extreme high density (col. 1, lines 36-39).

Also, Hong discloses external electrodes 5 exposed from the encapsulating resin 4, and the external electrodes 5 are formed on surfaces of the protruded portions 22 (col. 1, lines 44-54, and fig. 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form external electrodes exposed from the encapsulating resin, and the external electrodes are formed on surfaces of the protruded portions, as taught by Hong in order to make the thickness of the inner leads to be equal to the original lead frames and to minimize the partial etching area thereby preventing the poor connection property during metal wire-bonding process and to make the process of adjusting the bonding height a lot easier by preventing the metal wire to be exposed from the molding compound. Therefore, poor quality in the wire-bonding can be prevented (col. 2, lines 19-25, lines 52-53).

Regarding to claims 5, Chun-Jen discloses the semiconductor device wherein back faces of the inner leads are positioned substantially in the same plane as that of an external face of the encapsulating resin (fig. 1).

Regarding to claim 6, Chun-Jen discloses the semiconductor device wherein external end faces of the inner leads are positioned substantially in the same plane as that of external faces of the encapsulating resin (fig. 1).

Regarding to claim 7, figure 6 of Chun-Jen discloses a semiconductor device comprising a semiconductor chip 410/450; a plurality of inner leads 420 arranged along a periphery of the semiconductor chip 410/450; connecting members 430 for connecting the semiconductor chip 410/450 with the respective inner leads 420; an encapsulating resin 440 for encapsulating surfaces of the semiconductor chip 410/450 and the connecting members 430; the semiconductor chip includes a first semiconductor chip 410 and a second semiconductor chip 450, the second semiconductor chip 450 being smaller in size than the first semiconductor chip 410 and being stacked on a surface of the first semiconductor chip 410, each of the inner leads 420 extends across the periphery of the first semiconductor chip 410 from an internal side to an external side of the periphery, and includes a protruded portion 421 provided on a surface of the inner lead 420 on an external side relative to the periphery of the first semiconductor chip 410, the protruded portion 421 being protruded in a thickness direction, conductive bumps 460 that are formed as the connecting members of the first semiconductor chip 410 are connected with internal portions 422 of the respective inner leads 420, the internal portions 422 being positioned inward relative to the protruded portions 421, the second semiconductor chip 450 is disposed in a region surrounded by internal ends 422 of the inner leads 420, and is connected electrically with the first semiconductor chip 410 via conductive bumps 460, the encapsulating resin 440 encapsulates surfaces of the first and second semiconductor chips 410, 450 and the conductive bumps 460 (col. 4, lines 3-23).

Chun-Jen does not disclose a semiconductor chip on a surface of which a group of electrodes is provided; and external electrodes exposed from the encapsulating resin, and the external electrodes are formed on surfaces of the protruded portions, and tip ends of the external electrodes are protruded relative to a back face of the first semiconductor chip.

However, Sano discloses a semiconductor chip on a surface of which a group of electrodes 28 is provided (col. 4, lines 59-63, and fig. 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a semiconductor chip on a surface of which a group of electrodes 28 is provided, as taught by Sano in order to form the apparatus to be portable and smaller in size, many of the components are mounted in an extreme high density (col. 1, lines 36-39).

Also, Hong discloses the external electrodes 5 exposed from the encapsulating resin 4, and the external electrodes 5 are formed on surfaces of the protruded portions 22 (col. 1, lines 44-54, and fig. 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form external electrodes exposed from the encapsulating resin, and the external electrodes are formed on surfaces of the protruded portions, as taught by Hong in order to make the thickness of the inner leads to be equal to the original lead frames and to prevent poor quality in the wire-bonding (col. 2, lines 13-15 and lines 52-53).

Regarding to claim 8, figure 6 of Chun-Jen discloses the semiconductor device wherein an external face of the encapsulating resin 440, back faces of the inner leads 420, and a back face of the second semiconductor chip 450 are positioned substantially in the same plane.

Regarding to claim 9, figure 6 of Chun-Jen discloses the semiconductor device wherein external end faces of the inner leads 420 are positioned substantially in the same planes that contain external faces of the encapsulating resin 440.

Regarding to claims 10 and 14, figure 6 of Chun-Jen discloses the semiconductor device wherein each of the internal portion of the inner leads is inclined from a back face of the inner lead to protruded side of the protruded portion toward an internal end of the internal portion.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mai-Huong Tran whose telephone number is (571)272-1796. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MT
9/16/04

Mai-Huong Tran
Examiner
Art Unit 2818